

ADQ7–FWATD Datasheet



The Advanced Time Domain firmware option –FWATD equips ADQ7 with tools for sophisticated time-domain measurements. –FWATD contains four steps of noise suppression to reach extreme dynamic ranges:

- *Baseline stabilizer to eliminate long term fluctuations*
- *Linear noise suppression filter*
- *Non-linear noise suppression threshold*
- *Averaging for noise suppression by repetition*

Applications:

- *Scientific instruments*
- *Time-of-flight*
- *Mass spectrometry*
- *Electron paramagnetic resonance (EPR)*
- *Particle physics experiment*
- *Test & measurement*
- *Distributed fiber sensing*

ADQ7–FWATD Datasheet

Features

- 1 or 2 analog channels
- 10 or 5 GSPS per channel
- 14 bits vertical resolution
- External, internal, and SW trigger
- Bandwidth control filter
- Multi-unit synchronization
- Seamless streaming
- Safe scaled WFA for up to 262 144 records
- Record length up to 200 us

Advantages

- Advanced analog front-end, trigger functions, and high sampling rates for meeting systems requirements.
- Efficient utilization of dynamic range with an optional DC-offset.
- Signal conditioning through general FIR filter for noise reduction.
- Highly accurate and stable baseline provided for pulse applications.
- Threshold function to improve sparse pulses.
- Data rate reduction through accumulation of records in the FPGA.
- SP Devices' design services are available for fast integration to lower time-to-market.

Applications

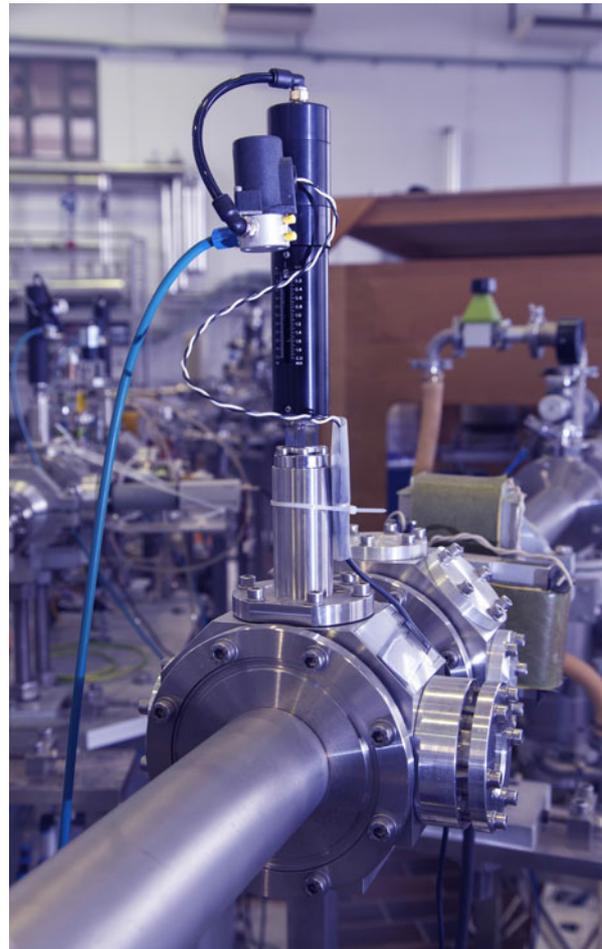
- Big Physics
- Time-of-flight
- Scientific instruments
- LIDAR
- RADAR
- Neutron time-of-flight

–FWATD is available for these ADQ7 modes:

ADQ7DC two-channel
ADQ7DC one-channel

–FWATD is available for form factors:

PCIe	USB3.0
10 GbE	Micro-TCA.4
PXIe	



Functional summary

The purpose of the –FWATD firmware option is to enhance signal to noise ratio in a pulse application measurement. The firmware contains four levels of noise suppression; baseline stabilization; linear filtering; non-linear threshold; and waveform averaging.

In an ADQ7 with several channels, there is one –FWATD unit per channel. They operate synchronously with the same settings on waveform size and number of accumulations. The filter and threshold properties are individual per channel.

For a high-level block diagram with the main functionality, see [Figure 1](#). The firmware consist of two parts; signal conditioning and accumulation. The signal conditioning contains baseline correction, filtering and threshold.

The accumulation finally accumulates records to reduce random noise.

Since the acquisition is dead-time free, the user has the freedom to continue accumulation in the user application, making the number of accumulations unlimited.

The baseline stabilizer gives a controlled reference level to enable accurate threshold. The DBS also reduce pattern noise from the digitizer.

Sampling at 10 GSPS means that the noise is in the band DC – 5 GHz. The signal however is in the band DC – 3 GHz due to the analog bandwidth limitation in the front-end. The general digital FIR filter can thus reduce the noise by a little over 2 dB without affecting the wanted signal.

The accumulator has a maximum length in number of samples. To increase the maximum available time measure, the sample skip is used.

The threshold function contains a filter in the threshold selection, which means that outliers from noise can be suppressed and not pass the threshold. This also increases the SNR.

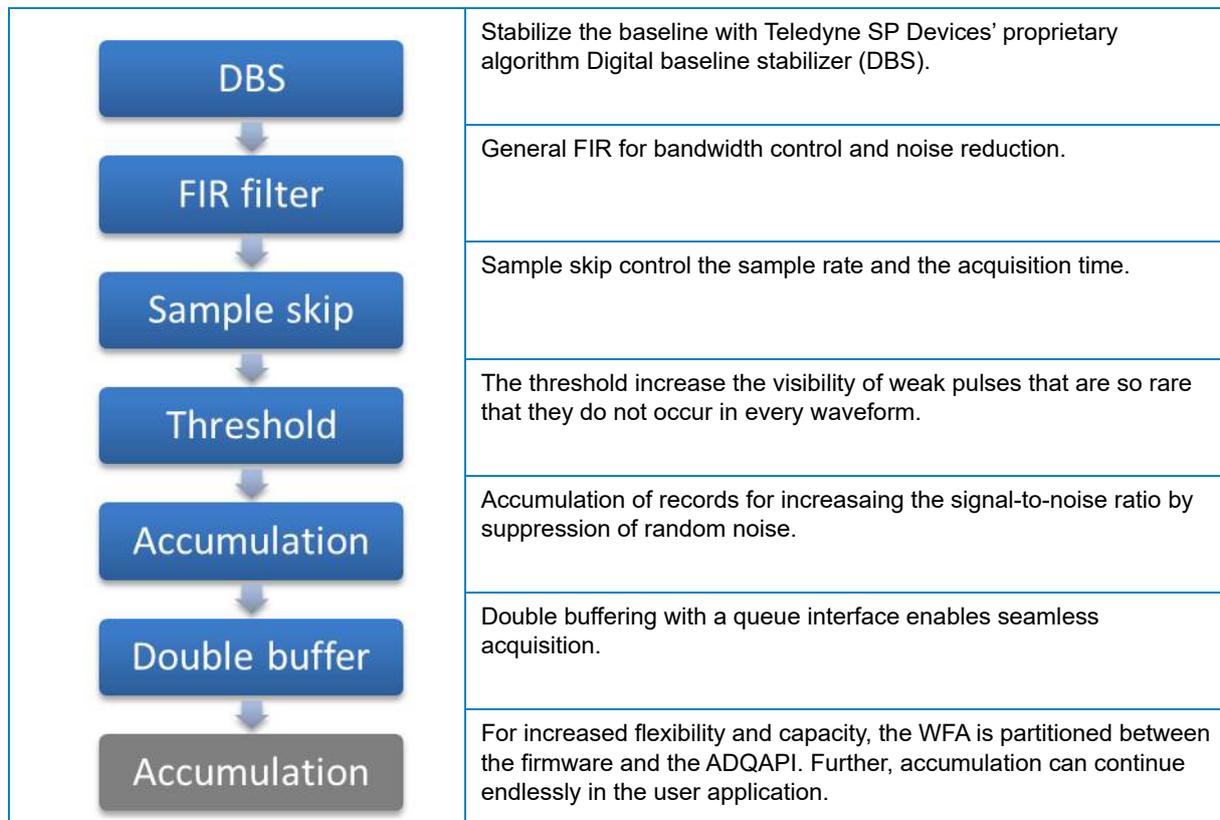


Figure 1: Block diagram of the main functionality of –FWATD.

Table 1: Triggers Settings

		–FWATD MIN	TYPICAL	MAX	DEFAULT
Trigger general					
Pre-trigger	[Samples]	0		16 000	0
Trigger delay	[Samples]	0	0	2^{32}	0
Rearm time	[ns]			32	
Eternal trigger (TRIG)					
Rime resolution	[ps]			50	
Internal trigger					
Trigger period	[Samples]	0		2^{32}	

Table 2: Definitions and acronyms

DEFINITION		COMMENT
Acronyms		
DBS	Digital baseline stabilizer	Teledyne SP Devices' proprietary IP
ADC	Analog-to-digital converter	
API	Application programming interface	
FWATD	Firmware for Teledyne SP Devices digitizers.	
FIR	Finite Impulse Response	
MSPS	10^6 samples per second	
GSPS	10^9 samples per second	
WFA	Waveform Accumulator/Accumulation	
SDK	Software development kit	
Definitions		
Header	Information about the record.	
Pulse	The samples between a trigger event and a reset event.	
Record	A set of data belonging to a trigger	The data is set consecutive samples
waveform	A set of data belonging to a trigger	Same as a record.

Software support

The –FWATD is supported by Windows and a number of Linux distributions. For a detailed list of operating systems, see (15-1494). The software development kit (SDK) contains the ADQAPI, drivers, examples and documentation.

Ordering information

The –FWATD can either be ordered together with an ADQ7, or separately, for loading into an existing unit. The –FWATD is delivered in two versions, one for operation in 5 GSPS dual channel mode

and one for operation in 10 GSPS single channel mode.

Technical data

Note that the 14-bit ADQ7 digitizer uses an MSB-aligned 16 bits data representation. The digital signal processing, for example DBS, will affect also the 2 LSBs making them non-zero. For the general specification of the ADQ7 digitizer, please refer to the ADQ7 datasheet (16-1692). Specification, definition and acronyms are listed in

Table 3: Settings

	–FWATD MIN	TYPICAL	MAX	DEFAULT
Data path Filter				
Filter length		17		
Filter coefficients	–2	0	$2 \cdot 2^{-14}$	0, center tap = 1
Filter coefficients resolution		2^{-14}		
Threshold Filter				
Filter length		17		
Filter coefficients	–2	0	$2 \cdot 2^{-14}$	0, center tap = 1
Filter coefficients resolution		2^{-14}		
WFA				
Number of accumulations	1		262 144 ¹	
Dead time waveform [ns]			32	
Dead time accumulation [ns]			32	
Waveform length [μs]	0.0032		200	
Length setting granularity [Samples]	32			
WFA 1-channel (10 GSPS)				
Waveform length [Samples]	32		2 097 152	
Length granularity [Samples]	32			
WFA 2-channel (5 GSPS)				
Waveform length [Samples]	16		1 048 576	
Length granularity [Samples]	16			
Registers				
DC-offset level [codes]	–32768	+/- 26000	+32767	0
DBS target [codes]	–32768	+/- 26000	+32767	0
Threshold level [codes]	–32768	+/- 26000 +/- T	+32767	0
Reference level [codes]	–32768	+/- 26000	+32767	0
DBS				
DC-offset level [codes]	–32768	+/- 26000	+32767	0
DBS target [codes]	–32768	+/- 26000	+32767	0
DBS accuracy [bits]		22		
DBS update rate [kHz]		1		0

1. Guaranteed safe scaling (32-bit accumulator).

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